Power converter

The invention relates to a power converter.

In power converters with a voltage doubler (see Fig. 1 for a typical application setup) an input mains voltage is rectified by a bridge rectifier D1-D4, and a remaining mains frequency ripple is filtered by means of electrolytic capacitors C1, C2. When Vac is about 110 V, switch S1 is closed, and when Vac is about 230 V, switch S1 is open. The midpoint of C1 and C2 is floating when S1 is open, possibly leading to an unbalance of the voltages across the capacitors C1 and C2 caused by the capacitor leakage current. This unbalance can lead to an overvoltage situation of C1 or C2. In theory the full DC voltage can be across one of the capacitors. For cost reasons capacitors are used having a maximum voltage of half the rectified DC voltage. One way to compensate for the leakage currents is the addition of resistors R1 and R2 in parallel to the capacitors C1, C2. A disadvantage of this approach is the inherent power dissipation. This jeopardizes low standby targets (e.g. Pin < 1 W when Po = 500 mW). Typically, a DC/DC converter followed by a load L are connected to an output of the bridge rectifier D1-D4.

An improvement of this circuit is proposed in EP-A-1315276. See Fig. 2 for the implementation. The proposed circuit in Fig. 2 reduces the dissipated power since the resistors R1 and R2 are regulated by transistors Q1 and Q2. Nevertheless the resistors R3, R4 and R5 are still conducting and adding to the input power consumption. The transistors Q1 and Q2 have to be high voltage switches, which will add significantly to the bill of materials compared to the traditional resistor solution presented in Fig. 1.

It is, inter alia, an object of the invention to provide an improved power converter. To this end, the invention provides a power converter as defined in claim 1. Advantageous embodiments are defined in the dependent claims.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawings:

Figs. 1-2 show prior art power supply circuits; and

Figs. 3-8 shows embodiments of a power supply circuit in accordance with the present invention.

Using the implementation of Fig. 3, in case of an overvoltage condition, zener diodes D5 and D6 protect the capacitors C1 and C2 by creating a parallel path for the leakage current. An advantage is that D5 and D6 are only conducting at the moment an overvoltage condition occurs (depending on the dimensioning of course), reducing the dissipation level to an absolute minimum since no resistors are involved. Also, the system costs of this embodiment are clearly lower than in the prior art of Fig. 2. The optional resistor R30 in the parallel path serves to limit the current though the zener diodes D5, D6. In an alternative to the embodiment shown in Fig. 3, the zener diodes may be connected each in the opposite direction with the arrows pointing towards each other.

In case C1 and C2 do not have the same value (e.g. not the same production batch) or the leakage currents are far from equal, the implementation of Fig. 4 can be used. In Fig. 4, diodes D7 and D8 are connected in parallel to the capacitors C1 and C2. The diodes D7 and D8 are connected such that normally no current flows through these diodes.

The embodiment of Fig. 5 provides the same function, although the overvoltage protection circuit is no longer short-circuited by the switch S1 if that switch is closed if an input AC voltage of about 110 V is applied, so that in this respect the embodiment of Fig. 5 is less favorable.

Fig. 6 shows a fully symmetrical alternative in which the overvoltage protection circuit comprises two branches, between a midpoint of the two capacitors and mutually different inputs of the rectifier circuit, each branch comprising a zener diode D5, D6, a resistor R30, R40, and a diode D9, D10. In this embodiment both capacitors C1, C2 are clamped simultaneously.

As shown in Figs. 7 and 8, resistors R50 and R60 may be connected in parallel to the zener diodes D5 and D6, respectively. This results in the advantage that the voltage at the midpoint between the capacitors C1, C2 is balanced at half the DC output voltage.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.